S.Y. Diploma : Sem. III  
[DE/ED/EI/EJ/EN/ET/EV/EX/IC/IE/IS/IU/MU]  
Principles of Digital Techniques  
Prelim Question Paper Solution  
[Marks : 100]

Instructions: 
(1) All questions are compulsory.  
(2) Illustrate your answers with neat sketches wherever necessary.  
(3) Figures to the right indicate full marks.  
(4) Assume suitable data if necessary.  
(5) Preferably, write the answers in sequential order.

1. (a) Attempt any SIX of the following: 
   (i) Convert $(48 \ BA)_{16}$ to a binary number. 
   (ii) Specify the function of following IC’s  
        IC 74138, IC 74139, IC 74154, IC 74155  
   (iii) Define fan in and propagation delay related to logic families.  
   (iv) Define the following terms:  
        (1) Propagation delay  
        (2) Fan-out  
   (v) Define:  
        (1) Minterm  
        (2) Maxterm  
   (vi) Draw the circuit diagram of D flip-flop using logic gate.  
   (vii) State the rules for BCD addition.  
   (viii) Differentiate between EPROM and EEPROM (any two points)  

   [12]

(b) Attempt any TWO of the following:  
   (i) Design a D- Flip Flop from a R-S Flip Flop.  
   (ii) Design a 3 : 8 decoder using Basic Logic Gates?  
   (iii) Perform the following BCD arithmetic:  
        (1) $(247)_{10} + (463)_{10}$  
        (2) $(42)_{10} - (27)_{10}$

   [8]

2. Attempt any FOUR of the following:  
   (a) What is race around condition in SR flip-flop? Describe the procedure to eliminate it.  
   (b) Prove that:  
        $ABC + ABD + \overline{ABC} + CD + B\overline{D} = B + CD$  
   (c) Design half Subtractor using logic gates.  
   (d) Design Delay Flip Flop, using RS Flip-flop.  
   (e) Subtract the given numbers using 1’s & 2’s complement method:  
        (i) 25-17  
        (ii) 17-25  
   (f) Minimize the following expression using K–map.  
        $F(A, B, C, D) = \Sigma m(0, 1, 2, 3, 4, 5, 7, 8, 9, 11, 14)$

   [16]

3. Attempt any FOUR of the following:  
   (a) Differentiate between Combinational Circuits and Sequential Circuits.  
   (b) Design the 3 bit Twisted ring counter. Explain its working with the help of wave forms.  
   (c) Differentiate between Synchronous and Asynchronous Counters?  
   (d) Give the comparison of CMOS and TTL families.  
   (e) What is necessity of De-MUX? Describe how de-multiplexer can be used as De-coder.  
   (f) Explain Master Slave JK Flip Flop, using NAND gates.

   [16]
4. Attempt any **FOUR** of the following:  
(a) Draw the circuit diagram of totem–pole TTL NAND gate and derive the relations for fanout and noise margins, power dissipation and propagation delay. Draw a transfer characteristic of TTL and explain the noise immunity.  
(b) Subtraction using 1’s and 2’s complement method:  
   (i) $(52)_{10} - (65)_{10}$  
   (ii) $(101011)_{2} - (11010)_{2}$  
(c) Design 1:8 demux using 1:2 demux only.  
(d) Minimize the following pos equation with k-map –  
   (i) $F = \sum m \{0, 3, 5, 6, 9, 10, 12, 15\}$.  
   (ii) $F = \sum m \{0,1,2,3,11,12,14,15\}$  
(e) Write the truth table of the given diagram.  

(f) Draw the block diagram of IC 7490 and explain its working as decade counter.  

5. Attempt any **FOUR** of the following:  
(a) Study the given diagram and  
   (i) Specify which type of counter it is  
   (ii) Design the truth table.  
(b) (i) Write the sop expression for the below circuit diagram.  
   (ii) Which is the fastest logic family out of all logic families and why?  
(c) Realize following equation using demultiplexer $f = \sum(0, 2, 5, 7, 8, 12, 15)$  
(d) (i) Add the following BCD no.  
   $(9)_{10} + (4)_{10}$  
   (ii) Subtract the following no using 10’s complement.  
   $(16)_{10} - (8)_{10}$  
(e) (i) Give any two differences between multiplexer and demultiplexer.  
   (ii) Draw CMOS inverter.  
(f) Realize Half Adder circuit using K-Map.
6. Attempt any **FOUR** of the following:  
   (a) Compare TTL, CMOS and ECL logic families.  
   (b) Give any four characteristics of ECL family.  
   (c) Draw the circuit diagram of 5-bit shift register and explain it with the help of timing diagram.  
   (d) Explain the method of operation of a Single Slope ADC?  
   (e) Draw the symbol for 2 input EX-NOR gate, write truth table & logical output equation.  
   (f) Draw the circuit and explain the principle of  
      (i) TTL NAND Gate  
      (ii) TTL Gate with Totem pole output